

Features

- Fast Read Access Time – 90 ns
- Dual Voltage Range Operation
 - Unregulated Battery Power Supply Range, 2.7V to 3.6V or Standard 5V \pm 10% Supply Range
- Compatible with JEDEC Standard AT27C010
- Low Power CMOS Operation
 - 20 μ A Max (Less than 1 μ A Typical) Standby for $V_{CC} = 3.6V$
 - 29 mW Max Active at 5 MHz for $V_{CC} = 3.6V$
- JEDEC Standard Packages
 - 32-lead PLCC
 - 32-lead TSOP
 - 32-lead VSOP
- High Reliability CMOS Technology
 - 2,000V ESD Protection
 - 200 mA Latchup Immunity
- Rapid Programming Algorithm – 100 μ s/Byte (Typical)
- CMOS and TTL Compatible Inputs and Outputs
 - JEDEC Standard for LVTTTL and LVBO
- Integrated Product Identification Code
- Industrial Temperature Range
- Green (Pb/Halide-free) Packaging Option

1. Description

The AT27BV010 is a high-performance, low-power, low-voltage 1,048,576-bit one-time programmable read-only memory (OTP EPROM) organized as 128K by 8 bits. It requires only one supply in the range of 2.7V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At $V_{CC} = 2.7V$, any byte can be accessed in less than 90 ns. With a typical power draw of only 18 mW at 5 MHz and $V_{CC} = 3V$, the AT27BV010 consumes less than one fifth the power of a standard 5V EPROM. Standby mode supply current is typically less than 1 μ A at 3V. The AT27BV010 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV010 is available in industry-standard JEDEC-approved one-time programmable (OTP) plastic PLCC, TSOP, and VSOP packages. All devices feature two-line control (\overline{CE} , \overline{OE}) to give designers the flexibility to prevent bus contention.

The AT27BV010 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at $V_{CC} = 5.0V$. At $V_{CC} = 2.7V$, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.



**1-Megabit
(128K x 8)
Unregulated
Battery-Voltage
OTP EPROM**

AT27BV010



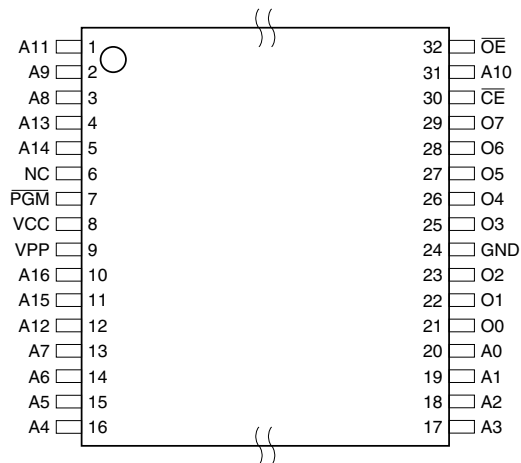


Atmel's AT27BV010 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 μ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages. The AT27BV010 programs exactly the same way as a standard 5V AT27C010 and uses the same programming equipment.

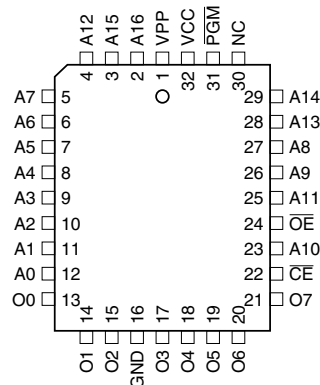
2. Pin Configurations

| Pin Name | Function |
|------------------|----------------|
| A0 - A16 | Addresses |
| O0 - O7 | Outputs |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| \overline{PGM} | Program Strobe |
| NC | No Connect |

2.1 32-lead TSOP/VSOP (Type 1) Top View



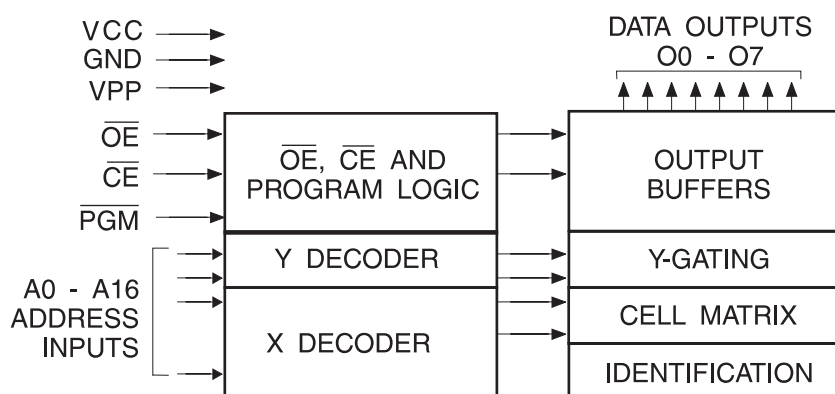
2.2 32-lead PLCC Top View



3. System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 μF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

4. Block Diagram



5. Absolute Maximum Ratings*

| | |
|---|--------------------------------|
| Temperature Under Bias..... | -40°C to +85°C |
| Storage Temperature | -65°C to +125°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V ⁽¹⁾ |
| Voltage on A9 with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |
| V_{PP} Supply Voltage with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75\text{V}$ DC which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

6. Operating Modes

| Mode/Pin | \overline{CE} | \overline{OE} | \overline{PGM} | Ai | V _{PP} | V _{CC} | Outputs |
|--|-----------------|-----------------|------------------|---|-----------------|-----------------|---------------------|
| Read ⁽²⁾ | V _{IL} | V _{IL} | X ⁽¹⁾ | Ai | X | V _{CC} | D _{OUT} |
| Output Disable ⁽²⁾ | X | V _{IH} | X | X | X | V _{CC} | High Z |
| Standby ⁽²⁾ | V _{IH} | X | X | X | X | V _{CC} | High Z |
| Rapid Program ⁽³⁾ | V _{IL} | V _{IH} | V _{IL} | Ai | V _{PP} | V _{CC} | D _{IN} |
| PGM Verify ⁽³⁾ | V _{IL} | V _{IL} | V _{IH} | Ai | V _{PP} | V _{CC} | D _{OUT} |
| PGM Inhibit ⁽³⁾ | V _{IH} | X | X | X | V _{PP} | V _{CC} | High Z |
| Product Identification ⁽³⁾⁽⁵⁾ | V _{IL} | V _{IL} | X | A9 = V _H ⁽⁴⁾ A0 = V _{IH} or V _{IL} A1 - A16 = V _{IL} | X | V _{CC} | Identification Code |

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Read, output disable, and standby modes require, $2.7V \leq V_{CC} \leq 3.6V$, or $4.5V \leq V_{CC} \leq 5.5V$.
 3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
 4. V_H = 12.0 ± 0.5V.
 5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

7. DC and AC Operating Conditions for Read Operation

| | AT27BV010-90 |
|---|--------------|
| Industrial Operating Temperature (Case) | -40°C - 85°C |
| V _{CC} Power Supply | 2.7V to 3.6V |
| | 5V ± 10% |

8. DC and Operating Characteristics for Read Operation

| Symbol | Parameter | Condition | Min | Max | Units |
|--------------------------------------|---|--|-----------------------|-----------------------|-------|
| V_{CC} = 2.7V to 3.6V | | | | | |
| I _{LI} | Input Load Current | V _{IN} = 0V to V _{CC} | | ±1 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} = 0V to V _{CC} | | ±5 | μA |
| I _{PP1} ⁽²⁾ | V _{PP} ⁽¹⁾ Read/Standby Current | V _{PP} = V _{CC} | | 10 | μA |
| I _{SB} | V _{CC} ⁽¹⁾ Standby Current | I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$ | | 20 | μA |
| | | I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V | | 100 | μA |
| I _{CC} | V _{CC} Active Current | f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$, V _{CC} = 3.6V | | 8 | mA |
| V _{IL} | Input Low Voltage | V _{CC} = 3.0 to 3.6V | -0.6 | 0.8 | V |
| | | V _{CC} = 2.7 to 3.6V | -0.6 | 0.2 x V _{CC} | V |
| V _{IH} | Input High Voltage | V _{CC} = 3.0 to 3.6V | 2.0 | V _{CC} + 0.5 | V |
| | | V _{CC} = 2.7 to 3.6V | 0.7 x V _{CC} | V _{CC} + 0.5 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.0 mA | | 0.4 | V |
| | | I _{OL} = 100 μA | | 0.2 | V |
| | | I _{OL} = 20 μA | | 0.1 | V |
| V _{OH} | Output High Voltage | I _{OH} = -2.0 mA | 2.4 | | V |
| | | I _{OH} = -100 μA | V _{CC} - 0.2 | | V |
| | | I _{OH} = -20 μA | V _{CC} - 0.1 | | V |
| V_{CC} = 4.5V to 5.5V | | | | | |
| I _{LI} | Input Load Current | V _{IN} = 0V to V _{CC} | | ±1 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} = 0V to V _{CC} | | ±5 | μA |
| I _{PP1} ⁽²⁾ | V _{PP} ⁽¹⁾ Read/Standby Current | V _{PP} = V _{CC} | | 10 | μA |
| I _{SB} | V _{CC} ⁽¹⁾ Standby Current | I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$ | | 100 | μA |
| | | I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V | | 1 | mA |
| I _{CC} | V _{CC} Active Current | f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$ | | 25 | mA |
| V _{IL} | Input Low Voltage | | -0.6 | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.0 | V _{CC} + 0.5 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA | | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -400 μA | 2.4 | | V |

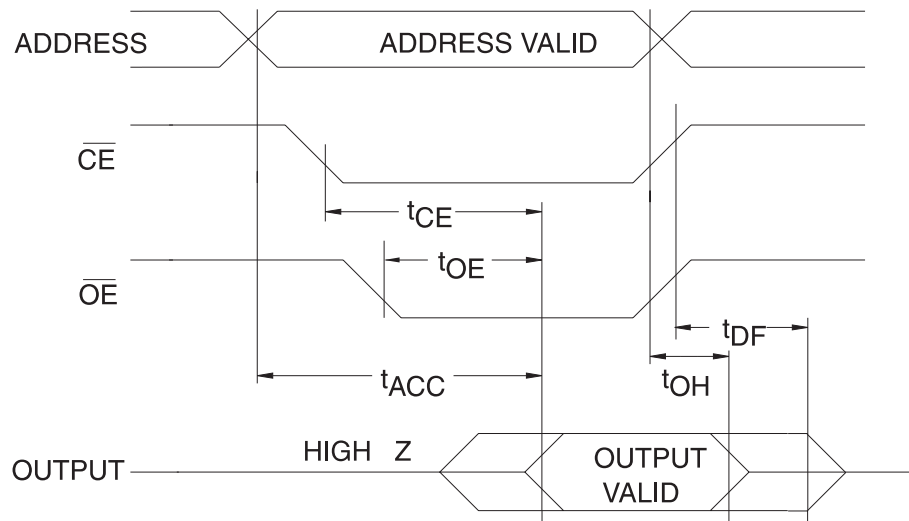
- Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

9. AC Characteristics for Read Operation

$V_{CC} = 2.7V$ to $3.6V$ and $4.5V$ to $5.5V$

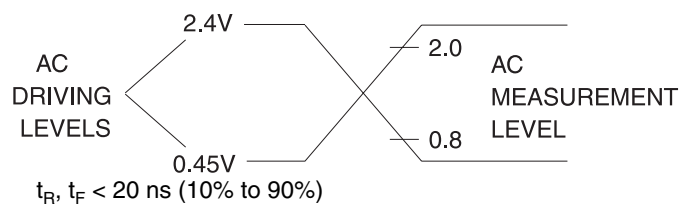
| Symbol | Parameter | Condition | -90 | | Units |
|-------------------|---|--|-----|-----|-------|
| | | | Min | Max | |
| $t_{ACC}^{(3)}$ | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ | | 90 | ns |
| $t_{CE}^{(2)}$ | \overline{CE} to Output Delay | $\overline{OE} = V_{IL}$ | | 90 | ns |
| $t_{OE}^{(2)(3)}$ | \overline{OE} to Output Delay | $\overline{CE} = V_{IL}$ | | 50 | ns |
| $t_{DF}^{(4)(5)}$ | \overline{OE} or \overline{CE} High to Output Float, Whichever Occurred First | | | 40 | ns |
| t_{OH} | Output Hold from Address, \overline{CE} or \overline{OE} , Whichever Occurred First | | 0 | | ns |

10. AC Waveforms for Read Operation⁽¹⁾

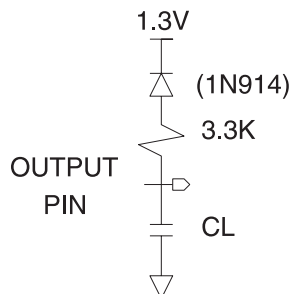


- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
 2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .
 3. \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC} .
 4. This parameter is only sampled and is not 100% tested.
 5. Output float is defined as the point when data is no longer driven.

11. Input Test Waveform and Measurement Level



12. Output Test Load



Note: CL = 100 pF including jig capacitance.

13. Pin Capacitance

f = 1 MHz, T = 25°C⁽¹⁾

| Symbol | Typ | Max | Units | Conditions |
|------------------|-----|-----|-------|-----------------------|
| C _{IN} | 4 | 8 | pF | V _{IN} = 0V |
| C _{OUT} | 8 | 12 | pF | V _{OUT} = 0V |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

15. DC Programming Characteristics

 $T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

| Symbol | Parameter | Test Conditions | Limits | | Units |
|-----------|--|---|--------|--------------|---------------|
| | | | Min | Max | |
| I_{LI} | Input Load Current | $V_{IN} = V_{IL}, V_{IH}$ | | ± 10 | μA |
| V_{IL} | Input Low Level | | -0.6 | 0.8 | V |
| V_{IH} | Input High Level | | 2.0 | $V_{CC} + 1$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1 \text{ mA}$ | | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -400 \mu\text{A}$ | 2.4 | | V |
| I_{CC2} | V_{CC} Supply Current (Program and Verify) | | | 40 | mA |
| I_{PP2} | V_{PP} Supply Current | $\overline{CE} = \overline{PGM} = V_{IL}$ | | 20 | mA |
| V_{ID} | A9 Product Identification Voltage | | 11.5 | 12.5 | V |

16. AC Programming Characteristics

 $T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.2\text{V}$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Limits | | Units |
|-----------|---|---|--------|-----|---------------|
| | | | Min | Max | |
| t_{AS} | Address Setup Time | Input Rise and Fall Times: (10% to 90%) 20 ns Input Pulse Levels: 0.45V to 2.4V Input Timing Reference Level: 0.8V to 2.0V Output Timing Reference Level: 0.8V to 2.0V | 2 | | μs |
| t_{CES} | \overline{CE} Setup Time | | 2 | | μs |
| t_{OES} | \overline{OE} Setup Time | | 2 | | μs |
| t_{DS} | Data Setup Time | | 2 | | μs |
| t_{AH} | Address Hold Time | | 0 | | μs |
| t_{DH} | Data Hold Time | | 2 | | μs |
| t_{DFP} | \overline{OE} High to Output Float Delay ⁽²⁾ | | 0 | 130 | ns |
| t_{VPS} | V_{PP} Setup Time | | 2 | | μs |
| t_{VCS} | V_{CC} Setup Time | | 2 | | μs |
| t_{PW} | \overline{PGM} Program Pulse Width ⁽³⁾ | | 95 | 105 | μs |
| t_{OE} | Data Valid from \overline{OE} | | 150 | ns | |
| t_{PRT} | V_{PP} Pulse Rise Time During Programming | 50 | | ns | |

- Notes:
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}
 - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
 - Program Pulse width tolerance is 100 $\mu\text{sec} \pm 5\%$.

17. Atmel's AT27BV010 Integrated Product Identification Code⁽¹⁾

| Codes | Pins | | | | | | | | | Hex Data |
|--------------|------|----|----|----|----|----|----|----|----|----------|
| | A0 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | |
| Manufacturer | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E |
| Device Type | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |

Note: 1. The AT27BV010 has the same Product Identification Code as the AT27C010. Both are programming compatible.

19. Ordering Information

19.1 Standard Package

| t _{ACC} (ns) | I _{CC} (mA) V _{CC} = 3.6V | | Ordering Code | Package | Operation Range |
|--------------------------|--|---------|--|----------------------------------|-------------------------------|
| | Active | Standby | | | |
| 90 | 8 | 0.02 | AT27BV010-90JI AT27BV010-90TI AT27BV010-90VI | 32J 32T 32V ⁽¹⁾ | Industrial (-40°C to 85°C) |

Note: Not recommended for new designs. Use Green package option.

19.2 Green Package (Pb/Halide-free)

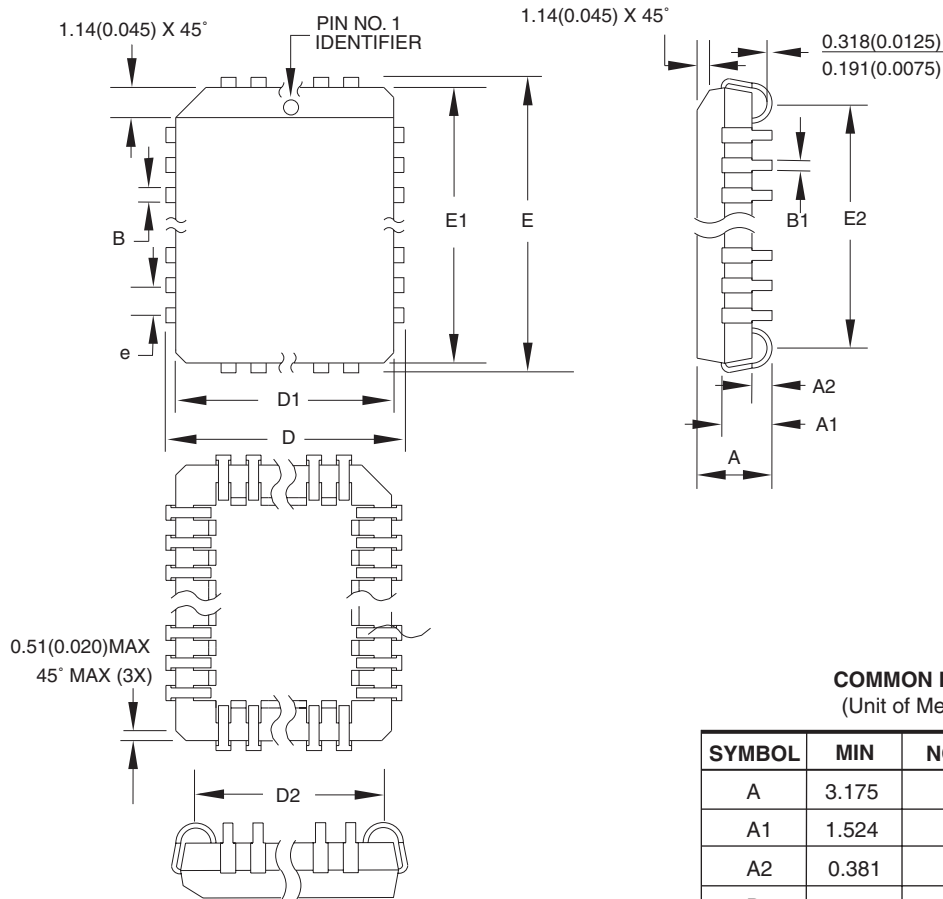
| t _{ACC} (ns) | I _{CC} (mA) V _{CC} = 3.6V | | Ordering Code | Package | Operation Range |
|--------------------------|--|---------|----------------------------------|------------|-------------------------------|
| | Active | Standby | | | |
| 90 | 8 | 0.02 | AT27BV010-90JU AT27BV010-90TU | 32J 32T | Industrial (-40°C to 85°C) |

Note: 1. The 32-lead VSOP package is not recommended for new designs.

| Package Type | |
|--------------|--|
| 32J | 32-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 32T | 32-lead, Plastic Thin Small Outline Package (TSOP) |
| 32V | 33-lead, Plastic Thin Small Outline Package (VSOP) |

20. Packaging Information

20.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | 3.175 | – | 3.556 | |
| A1 | 1.524 | – | 2.413 | |
| A2 | 0.381 | – | – | |
| D | 12.319 | – | 12.573 | |
| D1 | 11.354 | – | 11.506 | Note 2 |
| D2 | 9.906 | – | 10.922 | |
| E | 14.859 | – | 15.113 | |
| E1 | 13.894 | – | 14.046 | Note 2 |
| E2 | 12.471 | – | 13.487 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.